In the Specification:

Replace the paragraph beginning at page 7, line 2, with the following

--Fig. 1 is a block diagram of a circuit according to the invention;

Fig. ~~1a~~ 1A is a block diagram of an enhanced version of the circuit diagram shown in Fig. 1;

Fig. 2 is a block diagram of a phase-difference accumulator in the present circuit;

Fig. 3 is a block diagram of a sigma-delta modulator for phase-modulation attenuation;

Fig. 4 is a block diagram of the sigma-delta modulator for clock-rate conversion; and

Fig. 5 is a block diagram of a divider and multiplexer actuation circuit.--

Replace the paragraph beginning at page 16, line 16, with the following:

--Fig. ~~1a~~ 1A shows a detailed block diagram of the circuit according to the invention, in which the internal operating frequency is reduced in order to manage with a smaller number of high-speed components. To this end, the clock MCLK is divided by eight by a further divider 30, resulting in a clock at 2.048 or 1.544 MHz, respectively, instead of the MCLK clock of 16.384 or 12.352 MHz, respectively. The clock is then supplied as the in-use clock to the phase-difference accumulator 22 and to the sigma-delta modulator 26. The operating speed of the phase-difference transformer 24 is thus also automatically reduced to a corresponding extent. However, in this case, the output signals of the sigma-delta modulator 26 must be increased once again to the nominal frequency of 16.384 or 12.352 MHz, respectively, in order to actuate the divider 16. The COMMAND and DIRECTION signals are thus passed via an edge detector 32, which is connected between the sigma-delta modulator 26 and the divider 16, for matching to the clock MCLK. The edge detector is actuated by the signal MCLK.--

Replace the paragraph beginning at page 17, line 19, with the following:

--In situations in which SYNC ≠ 1/8 REF-CLK, the data rates must be converted from 2.048 to 1.544 MHz, or vice versa. To

this end, the sigma-delta modulator 20 for the clock-rate conversion is connected between the input of the signal SYNC and the phase comparator 18 as is shown in Figs. 1 and ~~1a~~ 1A. The configuration of the sigma-delta modulator is shown in more detail in Fig. 4. Clock-synchronous frequency division by a non-integer division factor in each case is thus required in this case.--

A3 Cont.